Weblab 2

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1 Characterization

See attached Figures 1 through 10.

2 Small Signal

I found the following equations in Howe and Sidoni and the course notes prepared by my TA.

$$R_{in} = r_\pi = \frac{\beta_f}{g_m}$$

$$R_{out} = r_{oPMOS} \| r_{oBJT}$$

$$A_V = g_m R_{out} = \frac{I_C}{V_{th}}(r_{oPMOS} \| r_{oBJT})$$

Assuming a worst case $R_{out} = 10K$, the requirement that $A_V > 100$ implies that $I_C > \frac{100V_{th}}{r_o}$ which simplifies to $I_C > 0.25mA$.

In order to satisfy the input impedance requirement that $r_{pi} < 10K$, we need to ensure that $g_m > \frac{\beta_f}{10K}$. Assuming a typical value for β_f of about 100, we need a value of $g_m > 0.01mho$. Looking at Graph 9, we can see that this condition is satisfied when $I_C > 0.2mA$. Graph 10 indicates that $r_\pi > 10K$ when $I_C > 0.25mA$.

In order to satisfy the output impedance requirement, we need to ensure that $r_{oPMOS} \| r_{oBJT} > 10K$. In the worst case, $r_{oPMOS} = r_{oBJT}$ and $R_out = \frac{r_{oPMOS}}{2}$. In order to meet our specification, even in the worst case, we need to make certain that $r_{oPMOS} > 20K$ and $r_{oBJT} > 20K$. Looking at Graph 7, we can see that $r_{oPMOS} > 20K$ only when $-I_D < 0.38mA$ for $V_{SD} = 1.5V$. Looking at Graph 8, we can see that $r_{oBJT} > 20K$ only when $I_C < 1.7mA$ for $V_{CE} = 1.5V$.

Combining all these constraints, we conclude that $0.25mA < I_C < 0.38mA$ in order to meet the specifications.

3 Bias Point Selection

We being by selecting an initial current $I_C = -I_D = 0.3mA$. Since our specification mandates that $V_{out} = 1.5V$, we can deduce that at the operating point, $V_{SD} = 1.5V$ and $V_{CE} = 1.5V$. Looking at Graph 2, we can see that in order to make $-I_D = 0.3mA$ at $V_{SD} = 1.5V$, we need to choose V_{SG} between 1.8 V and 1.4 V. We initially choose $V_{SG} = 1.6V$. Since $V_{SG} = V_S - V_G = 3 - V_B$, we conclude that our bias voltage $V_B = 1.4V$. Looking at Graph 1, we can see that in order to make $I_C = 0.3mA$ at $V_{CE} = 1.5V$, we need to set the base current $I_B = 2.4\mu A$. From Graph 3, we can see that this correspnds to a bias voltage $V_{Bias} = 0.71V$.

$$V_B = 1.4V$$

$$V_{Bias} = 0.71V$$

At these bias voltages, we can see by looking at Graph 10 that $r_\pi = 6K$. By looking at Graph 5, we can see that $r_{oPMOS} = 15K$ at the bias voltage I selected when $V_{SD} = 1.5V$. Graph 6 indicates that $r_{oBJT} = 120K$ for $V_{CE} = 1.5V$ when $I_B = 2.4\mu A$ which corresponds to the bias voltage I chose. Graph 9 indicates that at the given bias voltages, $g_m = 0.015mho$. Taken together, the measured data tells us the following information about how the amplifier would perform at the bias voltages I selected:

$$R_{in} = 6K$$

$$R_{out} = r_{oPMOS} \| r_{oBJT} = (15K) \| (120K) = 13.3K$$

$$A_V = g_m R_{out} = (0.015mho)(13.3K) = 200$$

$$V_{pp} = 2.25V - 0.75V = 1.5V$$

Because of measurement granularity, it is difficult to determine precisely V_{pp}, but we can extrapolate the available data to estimate a value. Since $r_{oPMOS} << r_{oBJT}$, the parallel combination of the two is dominated by r_{oPMOS}. Graph 6 indicates that r_{oBJT} does not vary much in the range of interest for the bias voltages I selected. Therefore, we can treat it as a constant and focus on how r_{oPMOS} affects the gain (and hence, the volage swing). Assuming $r_{oBJT} = 100K$, we see that in order for our gain to exceed 100 (given that g_m is more or less constant over the range of interest), we need to ensure that $r_{oPMOS} > 6.7K$. Graph 5 indicates that this should happen when $0.75V < V_{SD} < 2.25V$ which corresponds to $0.75V < V_{out} < 2.25V$.

V_{pp} is limited by the gain on both upswing and downswing. The gain is limited by the excessively low value of r_{oPMOS}, but since $r_{oPMOS} = \frac{1}{\lambda I_D}$, we can see that the underlying problem is that λ is too large. A smaller value of λ would increase the PMOS' output resistance and thereby increase the amplifier gain. Thus, the amplifier's limited V_{pp} is caused by excessive channel length modulation in the PMOS.

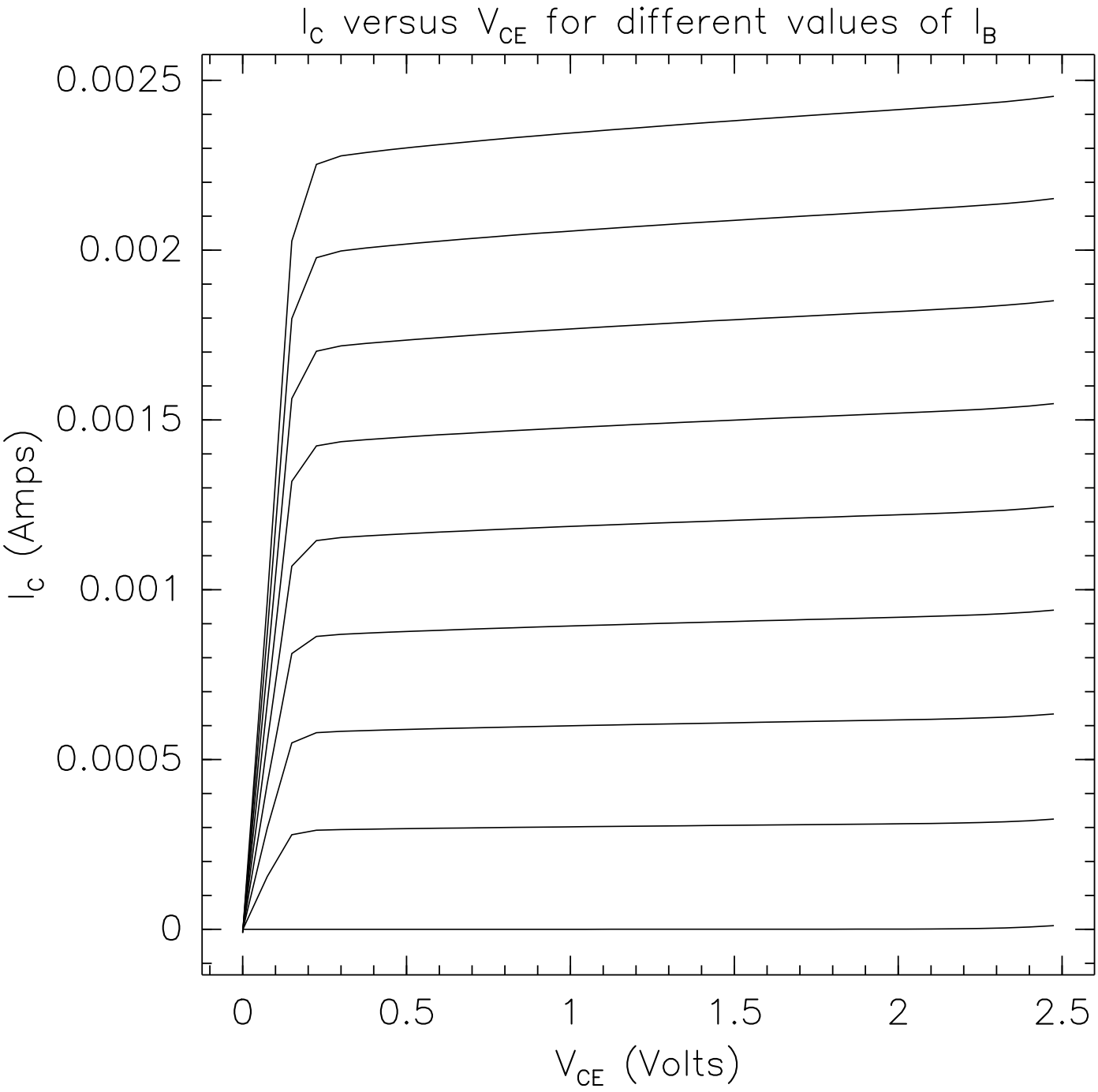
I_C versus V_{CE} for different values of I_B
0.0025
0.002
0.0015
0.001
0.0005
0
I_c (Amps)
0
0.5
1
1.5
2
2.5
V_{CE} (Volts)

Figure 1:

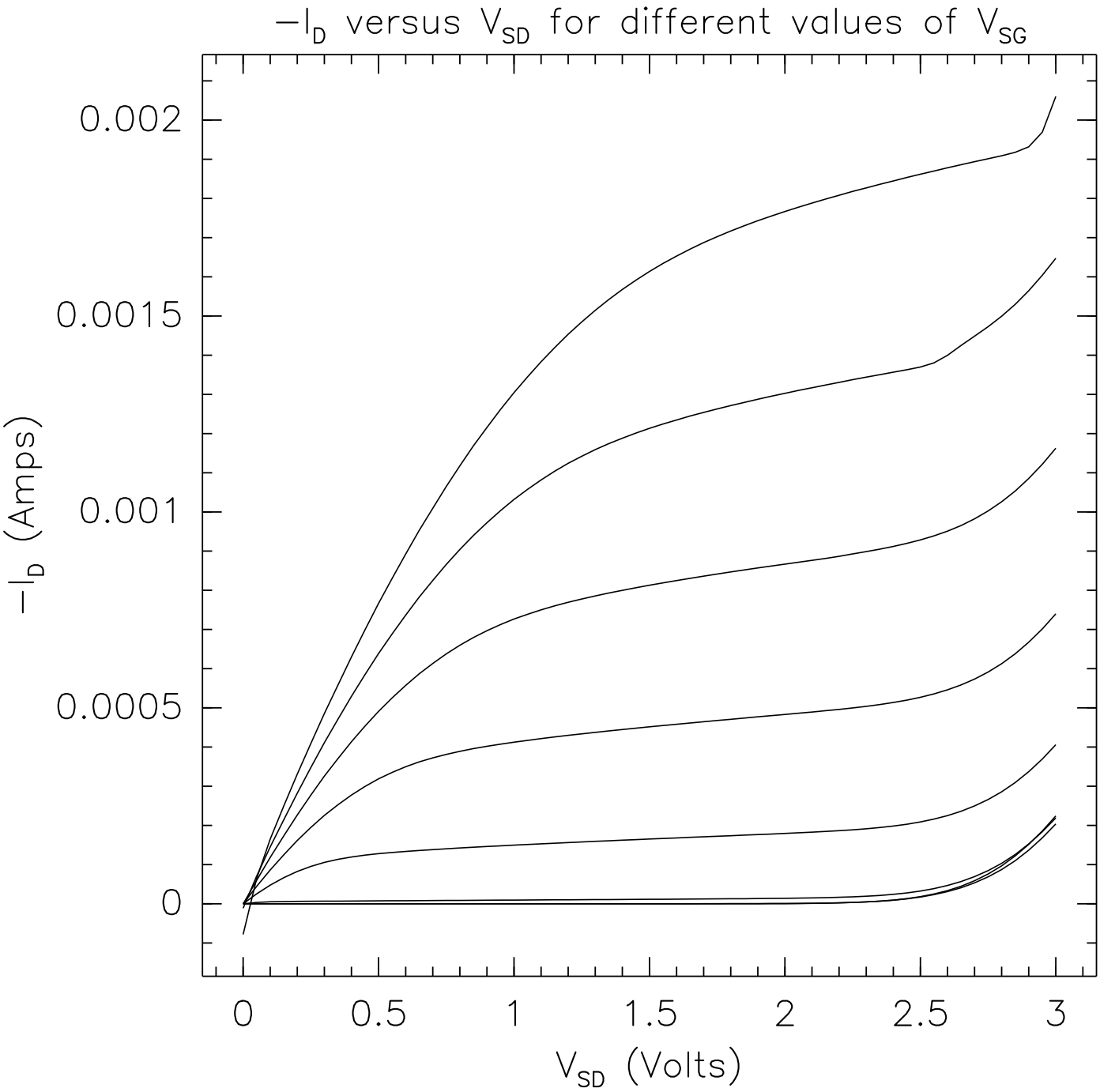
−I_D versus V_SD for different values of V_SG
0.002
0.0015
0.001
0.0005
0
−I_D (Amps)
0
0.5
1
1.5
2
2.5
3
V_SD (Volts)

Figure 2:

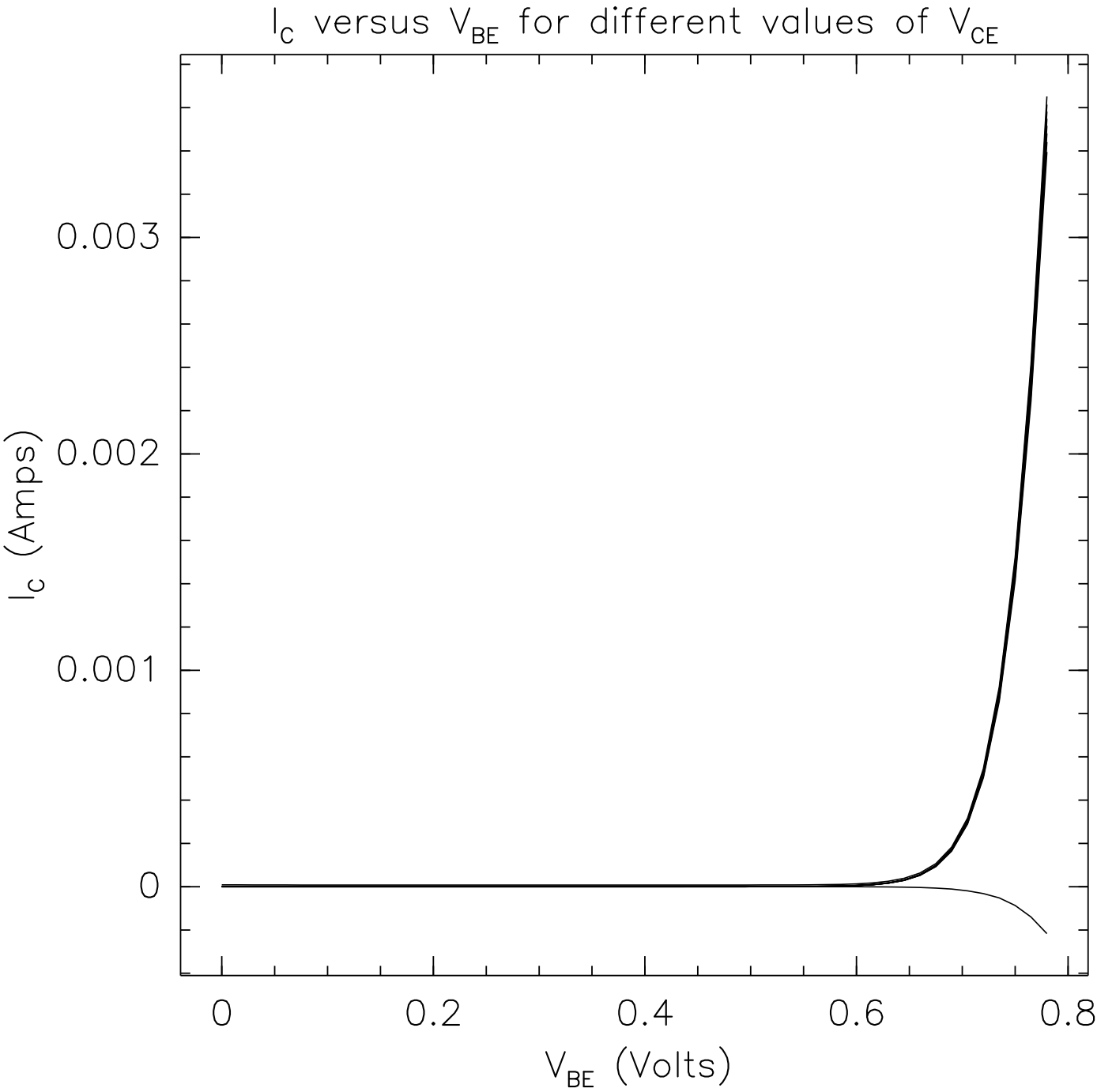
I_C versus V_{BE} for different values of V_{CE}
0.003
0.002
0.001
0
I_c (Amps)
0
0.2
0.4
0.6
0.8
V_{BE} (Volts)

Figure 3:

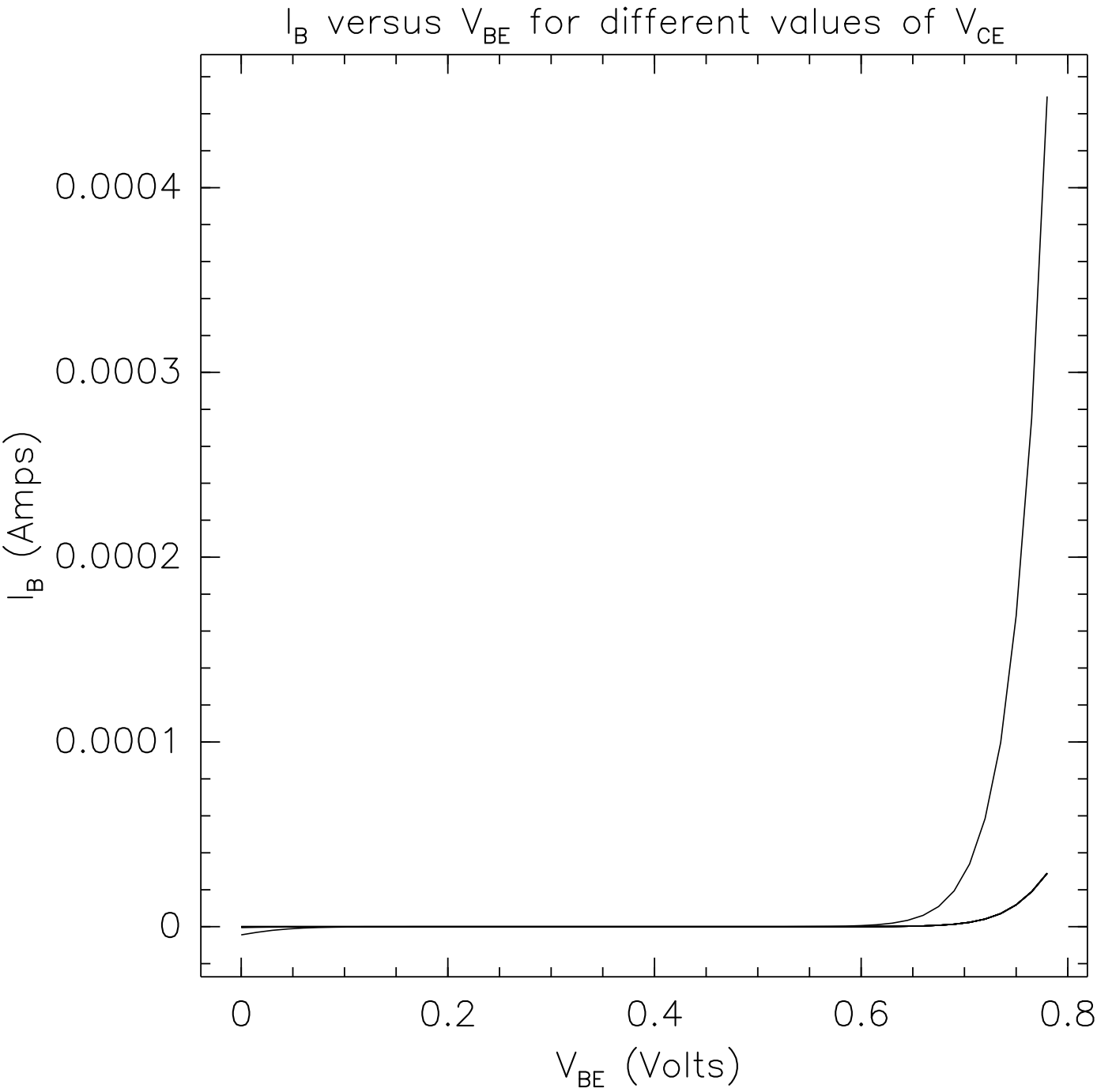
I_B versus V_{BE} for different values of V_{CE}
0.0004
0.0003
0.0002
0.0001
0
I_B (Amps)
0
0.2
0.4
0.6
0.8
V_{BE} (Volts)

Figure 4:

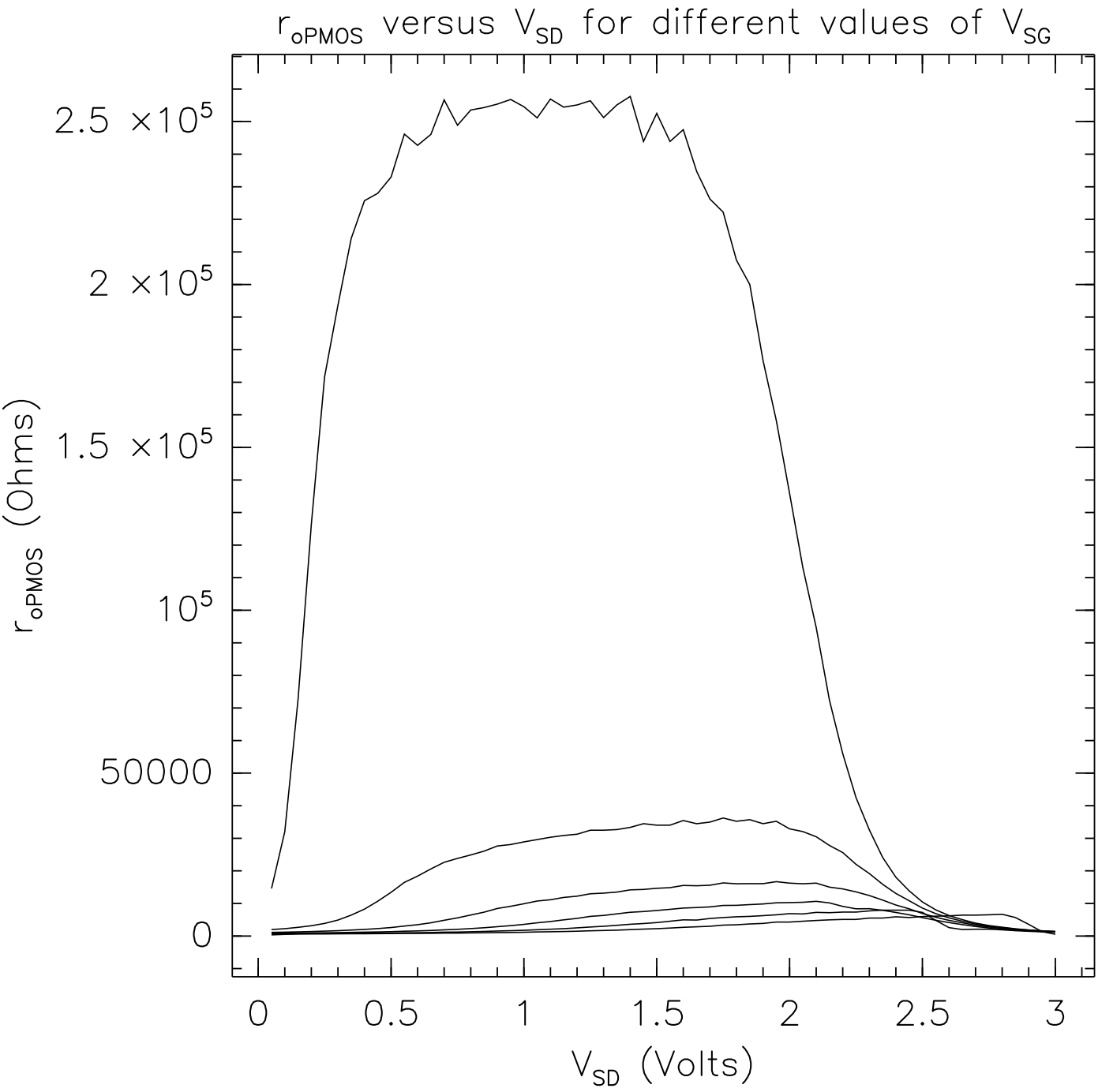
r_oPMOS versus V_SD for different values of V_SG
2.5 ×10^5
2 ×10^5
1.5 ×10^5
10^5
50000
0
r_oPMOS (Ohms)
0
0.5
1
1.5
2
2.5
3
V_SD (Volts)

Figure 5:

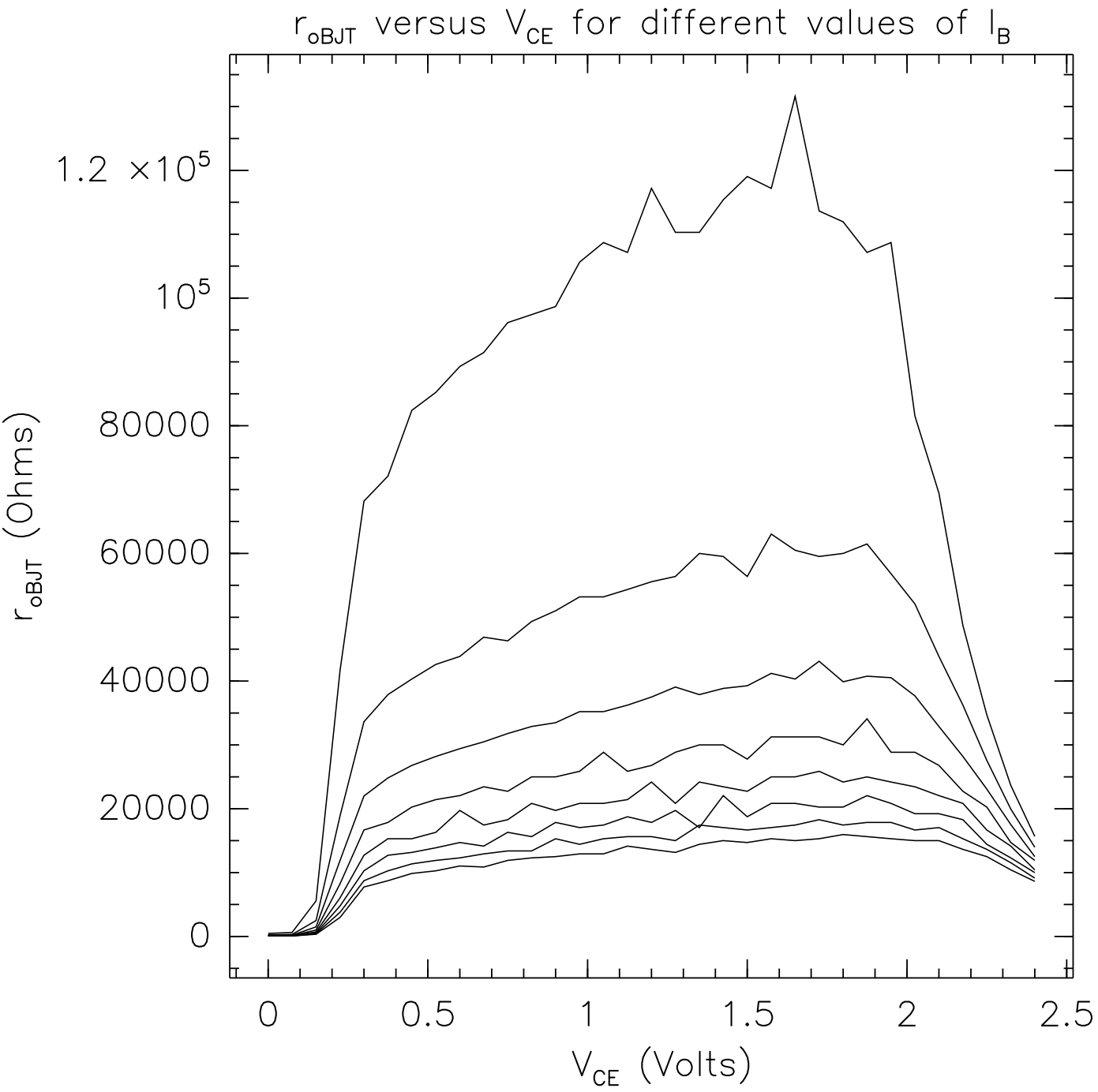
r_oBJT versus V_CE for different values of I_B
1.2 ×10^5
10^5
80000
60000
40000
20000
0
r_oBJT (Ohms)
0
0.5
1
1.5
2
2.5
V_CE (Volts)

Figure 6:

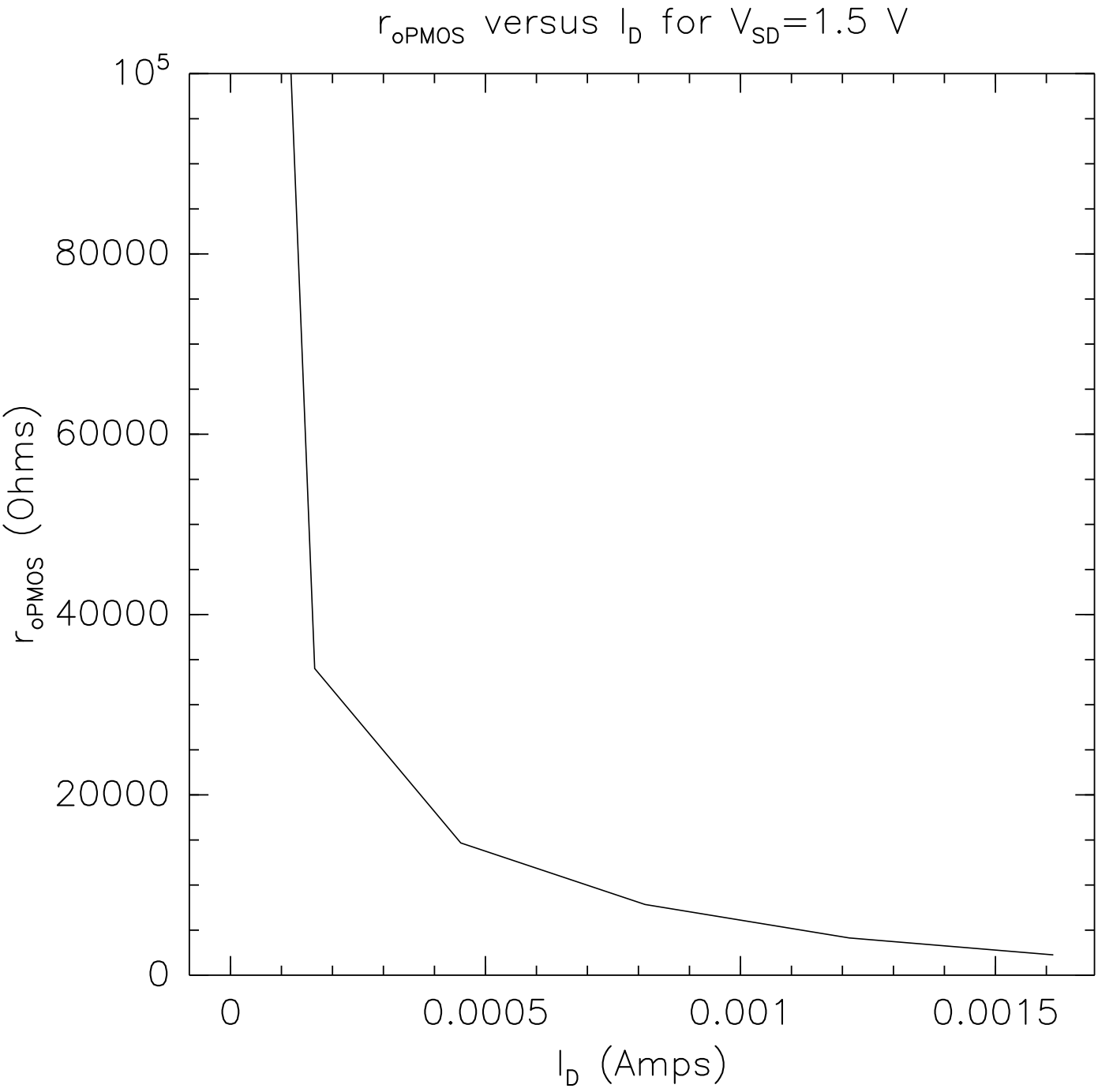
r_{oPMOS} versus I_D for V_{SD}=1.5 V
10^5
80000
60000
40000
20000
0
r_{oPMOS} (Ohms)
0
0.0005
0.001
0.0015
I_D (Amps)

Figure 7:

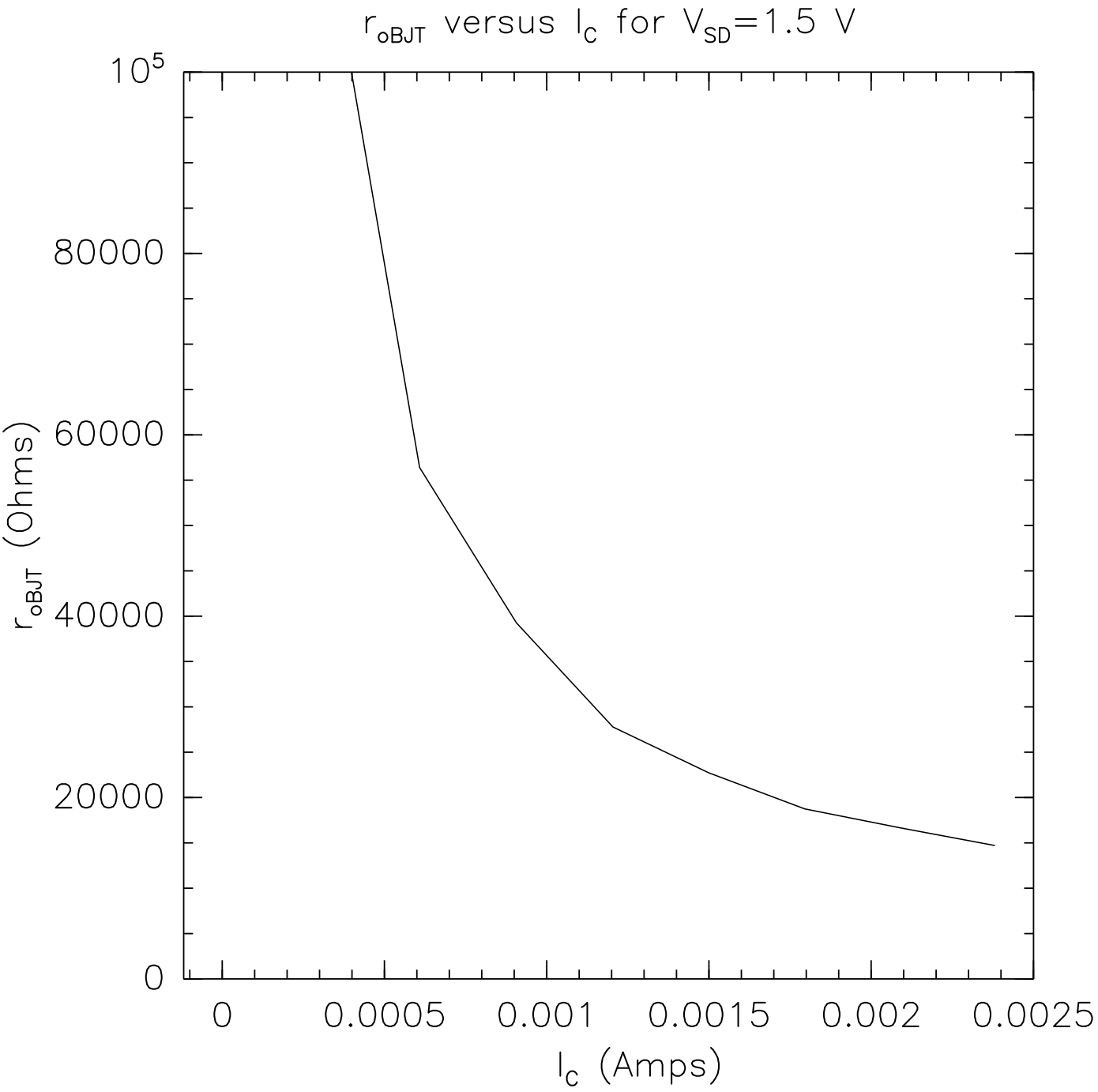
r_{oBJT} versus I_C for V_{SD}=1.5 V
10^5
80000
60000
40000
20000
0
r_{oBJT} (Ohms)
0
0.0005
0.001
0.0015
0.002
0.0025
I_C (Amps)

Figure 8:

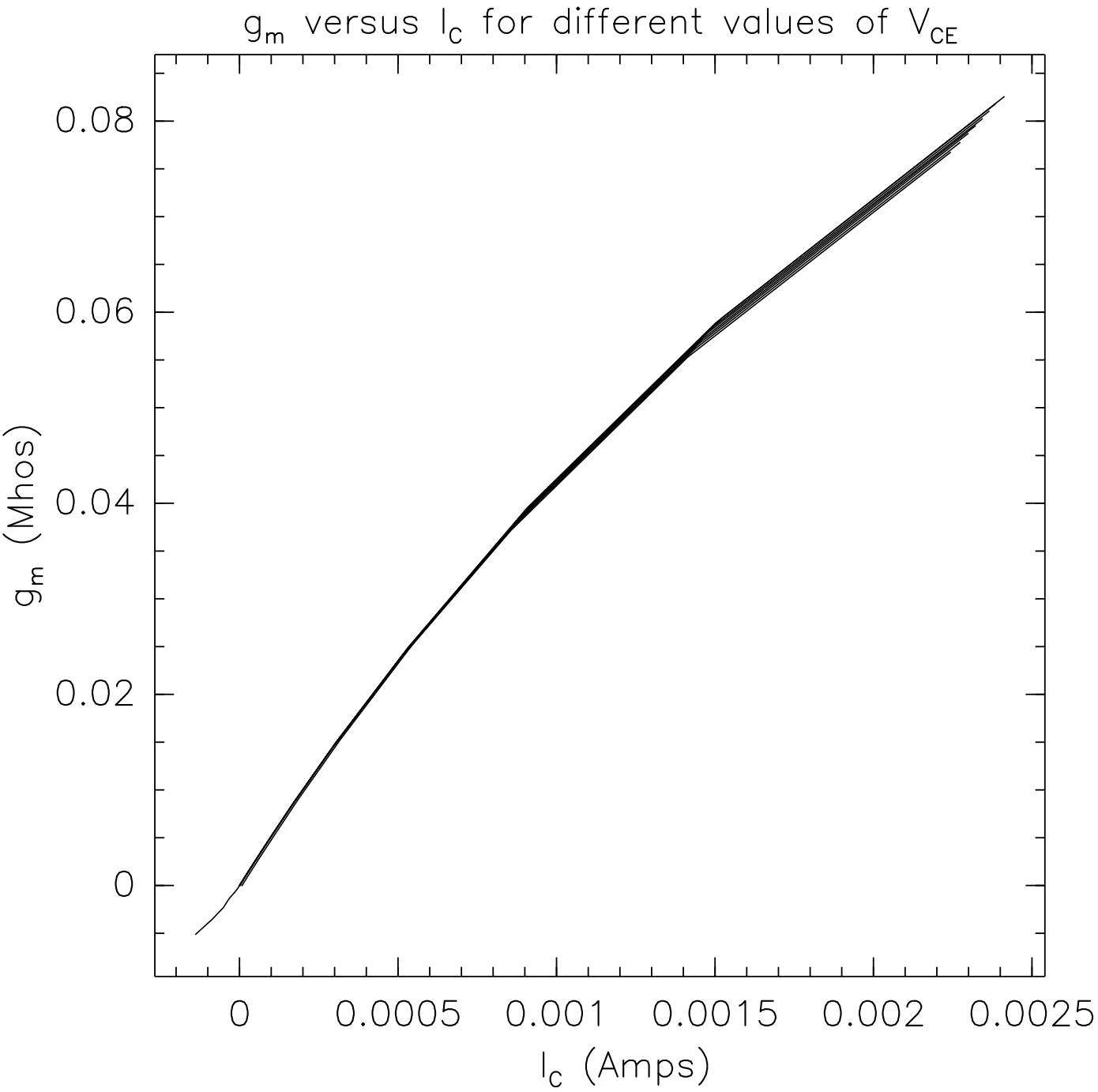
g_m versus I_C for different values of V_{CE}
0.08
0.06
0.04
0.02
0
g_m (Mhos)
0
0.0005
0.001
0.0015
0.002
0.0025
I_C (Amps)

Figure 9:

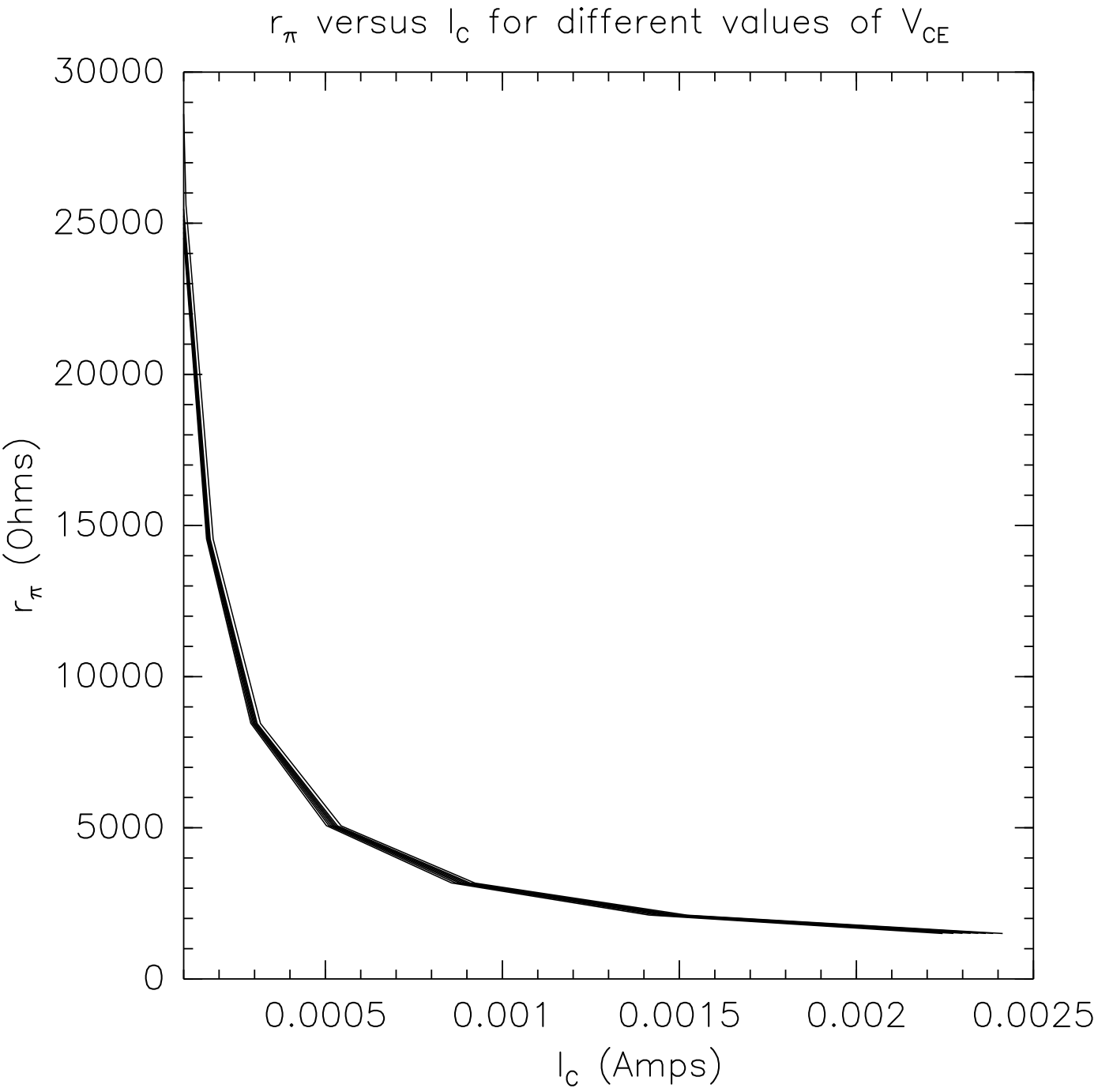
r_π versus I_C for different values of V_{CE}
30000
25000
20000
15000
10000
5000
0
r_π (Ohms)
0.0005
0.001
0.0015
0.002
0.0025
I_C (Amps)

Figure 10: